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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/874,173	Applicant(s) GOLD ET AL.	
	Examiner David J. Huisman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #2. IDS as received on 11/18/2002.

Specification

3. The abstract is objected to because it is too short and it repeats information given in the title. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The disclosure is objected to because of the following informalities: On page 7, line 5, replace "as R3" with --in R3--. On page 7, line 22, remove the period after "soon-to-be-free".

On page 10, line 4, replace "register" with --registers--. On page 10, line 28, remove one of the "s after "46".

Appropriate correction is required.

Drawings

5. The drawings are objected to because of the following minor informalities: In Fig.2A, replace "Architectural Registers numbers 21B" with --Architectural register numbers 21B-- and replace "soon to be free" with --soon-to-be-free--. In Fig.2B, replace "Architectural Registers numbers 21B" with --Architectural register numbers 21B-- and replace "soon to be free" with --soon-to-be-free--. In Fig.3, replace all occurrences of "FPRL" with --FPRA--, all occurrences of "RPA" with --APRM--, and all occurrences of "RPM" with --RPRM--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claim 21 must be shown or the feature(s) canceled from the claim(s). More specifically, the examiner is unable to find a drawing showing transferring a register assignment from the first structure to the second structure upon retirement. The drawings currently show three structures, where upon retirement, a register assignment is transferred from a third structure (APRM) to the second structure. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claim 10 is objected to because of the following informalities: Please insert a comma after "registers" in line 1. Also, please insert another line-break between lines 4 and 5 on page 14. Finally, in the second to last line of claim 10, insert --identifying-- after "information". Appropriate correction is required.

8. Claim 21 is objected to because of the following informalities: Please insert a period at the end of the claim. Also, insert a comma after "registers" in line 1.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 5 and 14 recite the limitation "the mappings" in line 3. There is insufficient antecedent basis for this limitation in the claims. For purposes of this examination, "the mappings" will be interpreted as simply mapping physical registers to some other value.

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not describe the transfer of physical register assignments from the first structure to the second structure as claimed in claim 21. The examiner is not clear as to how this is possible because the first structure does not store physical register *assignments*. Instead, the first structure, according to claim 21, stores information identifying available physical registers, not register assignments. Therefore, register assignments cannot be transferred from the first to second structure as claimed. And, the specification fails to enable such a transfer.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-3, 5, 7-8, 10-12, 14, 17, 19, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Faraydon, EP Publication Number 0600611A2 (as disclosed by applicant and herein referred to as Faraydon).

15. Referring to claim 1, Faraydon has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.6, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For instance, when the lock bit = 1, the corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) providing a third structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03). These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

d) transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure.

e) when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said physical register as available to said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

16. Referring to claim 2, Faraydon has taught a method as described in claim 1. Faraydon has further taught storing mappings of logical registers to said plurality of physical registers. See the CVT tables and the Rename tables. Note that physical/logical mappings are stored in these tables. For instance, looking at Fig.13, in Rename 2, logical register 00 is assigned to physical register 00, logical register 01 is assigned to physical register 01, logical register 02 is assigned to physical register 02, and logical register 03 is assigned to physical register 04. The CVT tables hold similar mappings.

17. Referring to claim 3, Faraydon has taught a method as described in claim 2. Faraydon has further taught that the microprocessor is comprised of a memory array and wherein said

method further comprises the step of storing said mappings to the memory array. From Fig.13, the mappings are stored in the CVT tables and the Rename tables. As can be seen from the figure, the CVT tables are shown as a 4x3 array (4 rows, 3 columns). Likewise, the Rename tables are essentially 4x1 arrays (4 rows, 1 column).

18. Referring to claim 5, Faraydon has taught a method as described in claim 1. Faraydon has further taught that contents of said first structure, second structure, and third structure of available registers are self-initialized to store the mappings of said physical registers. See Fig.7, note that the physical registers in the first structure are mapped to lock bit values and actual data values. In the second structure, physical registers are mapped to flag values (000), which are changed as instructions are executed. See Fig.9, for instance, and note that the initial value of 000 has been changed to 100. Finally, the third structure (Rename 2) is initialized with mappings of physical to logical registers.

19. Referring to claim 7, Faraydon has taught a method as described in claim 1. Faraydon has further taught the step of detecting whether said assigned available physical registers are being utilized by said microprocessor for execution. If an available physical register is assigned to be a destination for an instruction, then that register is detected as being utilized during execution. That is, the processor will detect that register X is the destination and therefore, the result of the instruction will be written there.

20. Referring to claim 8, Faraydon has taught a method as described in claim 1. Faraydon has further taught that said method is performed by hardware. See Fig.2 and Fig.6+. Note that the method is performed by hardware.

21. Referring to claim 10, Faraydon has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned to a plurality of destination operands for instructions executing on the microprocessor, said plurality of destination operands identifying where data resulting from an operation is to be stored. See Fig.6 and Fig.6+, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For instance, when the lock bit = 1, the corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned to one of said plurality of destination operands for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) providing a third structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03). These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add

instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

d) transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure.

e) and when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available to said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

22. Referring to claim 11, Faraydon has taught a method as described in claim 10. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

23. Referring to claim 12, Faraydon has taught a method as described in claim 11. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

24. Referring to claim 14, Faraydon has taught a method as described in claim 10. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

25. Referring to claim 17, Faraydon has taught a method as described in claim 10. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

26. Referring to claim 19, Faraydon has taught a microprocessor system with a plurality of physical registers for managing a plurality of physical register assignments comprising:

a) a first module for providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.6, and note the table made up of components 16 and 17. Each row corresponds to a different physical register and the lock bit for each register determines whether or not that particular register is free to be assigned as a destination operand. For instance, when the lock bit = 1, the corresponding register is not free to be assigned as a destination for an instruction. However, when the lock bit = 0, the register is free.

b) a second module for storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. See Fig.8 and notice that CVT 0 is this second structure. More specifically, a physical register is assigned as a destination operand for the Add instruction. This is accomplished by setting the lock bit for register 04 in the first structure to a value of 1. Then, in the second structure (CVT 0), physical register 04 is assigned to logical register 03 (the destination of the Add instruction).

c) a third module for providing a third structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03).

These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

d) a first interface for transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.11 and Fig.12 and notice the communication between the second structure (CVT 0) and the third structure (Rename 2). When the instruction retires, the assignment is transferred from the second to third structure. That is, the mapping of register 03 to 04 in the second structure is transferred to the third structure.

e) a second interface for, when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available to said first structure. When a subsequent instruction is assigned the selected physical register, the lock bit will be set in the first structure, thereby indicating that the selected register is made available to the subsequent instruction. In order to set this lock bit, a data value of 1 (information) must be transferred to the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

27. Referring to claim 21, Faraydon has taught in a microprocessor having a plurality of physical registers a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned to a plurality of destination operands for instructions executing on the

microprocessor, said plurality of destination operands identifying where data resulting from an operation is to be stored. See Fig.8 and notice that CVT 0 is this first structure. Note that this structure (along with CVT 1) list registers 04-11, which are physical registers that are available for assignment. Furthermore, it should be noticed that register 04 is assigned the logical name 03.

b) providing a second structure for holding information regarding available physical registers not utilized during execution of instructions. See Fig.8, and notice the "Rename 2" table. In this particular figure, this table specifies 4 physical registers (00-03). These registers are free since they have a lock bit of 0. And, registers 00 and 03 are not utilized during execution of the Add instruction (note that registers 01 and 02 are utilized as sources and 04 is used as the destination, not 03). Therefore, the third structure holds information regarding available registers not utilized during execution.

c) transferring said physical register assignment of said selected physical register from said first structure to said second structure after retirement of said selected instruction.

d) and when said selected physical register is assigned as a destination operand for a subsequent instruction, transferring information identifying said physical register as available to said first structure. When the same physical location is used in the future, mapping information which assigns the physical register to a logical register will be transferred to the first structure. This, in essence, implies that the register is available because if the register is not available, it will not be stored in the first structure. It should be realized that applicant does not specify where this information is transferred from, nor what this information comprises.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 4, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above.

30. Referring to claim 4, Faraydon has taught a method as described in claim 1. Faraydon has not taught that said microprocessor simultaneously executes multiple threads. However, Official Notice is taken that threads and the ability of a processor to execute multiple threads in parallel (simultaneously) is well known and expected in the art. Threads are separate independent sections of code which perform a particular task. They are advantageous in that they hide the latency of a processor while performing a long-latency instruction such as a load from main memory. Instead of simply stalling and waiting for the result, the processor can switch to another thread and continue executing. In addition, when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially. As a result, in order to increase the efficiency of the system, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Faraydon to execute multiple threads simultaneously.

31. Referring to claim 13, Faraydon has taught a method as described in claim 10. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

32. Referring to claim 20, Faraydon has taught a method as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

33. Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above, in view of Yung et al., U.S. Patent No. 5,546,554 (as disclosed by applicant and herein referred to as Yung).

34. Referring to claim 6, Faraydon has taught a method as described in claim 1. Faraydon has not taught that contents of said assigned available physical registers are flushed from said assigned available physical registers. However, Yung has taught such a concept. See column 12, line 26, to column 13, line 5, and Fig.13b, 14b, and 15b. Note that if an instruction causes an exception, it along with all of the younger instructions must be flushed, including their results, so that the system can be restored to the state prior to the exception. If this flushing does not occur, then the system will contain corrupt/incorrect data which would cause the program to yield incorrect results. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Faraydon in view of Yung such that contents of assigned physical registers in Faraydon are flushed when exceptions occur.

35. Referring to claim 15, Faraydon has taught a method as described in claim 10. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

36. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraydon, as applied above, in view of Tanenbaum, Structured Computer Organization, 2nd Edition, 1984, page 11 (herein referred to as Tanenbaum).

37. Referring to claim 18, Faraydon has taught a method as described in claim 1. Although Faraydon has taught that said method is performed by hardware (Fig.2 and Fig.6+), Faraydon has not explicitly taught that said method is performed by software. However, Tanenbaum has taught that hardware and software are logically equivalent. See page 11. Therefore, a person of ordinary skill in the art would've recognized that the function performed by the hardware could be implemented in software and vice-versa. As Tanenbaum has further suggested, the choice between hardware and software implementations is based on the designer's needs as well as cost, speed, reliability, and frequency. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Faraydon such that software performs the method instead of hardware.

38. Referring to claim 18, Faraydon has taught a method as described in claim 10. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Gaertner et al., U.S. Patent No. 6,108,771, has taught register renaming with a pool of physical registers. Free and active register structures are disclosed.

Jourdan et al., U.S. Patent No. 6,505,293, has taught register renaming to optimize identical register values. Prior art has been disclosed which shows data transfer between multiple register structures, i.e., a free register list, a register mapping table, and an active register list.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
June 2, 2004

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